[0021] In a further embodiment, the high-k material portion comprises one of HfO_2, ZrO_2, La_2O_3, Al_2O_3, TiO_2, $SrTiO_3$, $LaAlO_3$, Y_2O_3, HfO_xN_y, ZrO_xN_y, $La_2O_xN_y$, $Al_2O_xN_y$, TiO_xN_y, $SrTiO_xN_y$, $LaAlO_xN_y$, $Y_2O_xN_y$, a silicate thereof, and an alloy thereof, wherein each value of x is independently from about 0.5 to about 3 and each value of y is independently from 0 to about 2.

[0022] In an even further embodiment, the metal gate portion comprises one of TiN, ZrN, HfN, VN, NbN, TaN, WN, TiAlN, TaCN, W, Ta, Ti, other conductive refractory metal nitrides, and an alloy thereof.

[0023] In a yet further embodiment, the high-k material metal gate structure further includes a second doped semiconductor portion comprising a doped semiconductor and vertically abutting the metal gate portion.

[0024] In a still further embodiment, the semiconductor gate structure further includes a third doped semiconductor portion comprising the doped semiconductor and vertically abutting the doped semiconductor portion.

[0025] In a still yet further embodiment, the third doped semiconductor portion and the doped semiconductor portion comprise different materials.

[0026] According to another aspect of the present invention, a method of forming a semiconductor structure is provided, which comprises:

[0027] forming a first gate structure and a second gate structure on a semiconductor substrate, wherein the first gate structure includes a high dielectric constant (high-k) material portion having a dielectric constant greater than 8.0, and wherein the second gate structure includes a semiconductor oxide containing gate dielectric portion having a dielectric constant less than 8.0;

[0028] forming an oxygen-impermeable dielectric layer over the first gate structure and the second gate structure; and

[0029] removing a first portion of the oxygen-impermeable dielectric layer over the second gate structure, while protecting a second portion the oxygen-impermeable dielectric layer over the first gate structure.

[0030] In one embodiment, the method further comprises forming a low-k spacer having a dielectric constant less than 4.0 directly on sidewalls of the second gate stack and the second portion of the oxygen-impermeable dielectric layer.

[0031] In another embodiment, the method further comprises forming another low-k spacer having a dielectric constant less than 4.0 directly on sidewalls of the oxygen-impermeable dielectric layer over the first gate structure.

[0032] In even another embodiment, the method further comprises etching the second portion of the oxygen-impermeable dielectric layer to form an oxygen-impermeable dielectric spacer.

[0033] In yet another embodiment, the oxygen-impermeable dielectric spacer comprises silicon nitride and has an L-shaped cross-sectional area.

[0034] In still another embodiment, the first gate structure further includes a metal gate portion comprising a metal and vertically abutting the high-k material portion, and the second gate structure further includes a first doped semiconductor portion comprising a doped semiconductor material and vertically abutting the semiconductor oxide containing gate dielectric portion.

[0035] In still yet another embodiment, the first gate structure further includes a chemical oxide portion vertically abutting the high-k material portion and the semiconductor substrate and comprising an oxide of a semiconductor material of the semiconductor substrate.

[0036] In a further embodiment, the method further comprises:

[0037] forming a second doped semiconductor portion directly on the metal gate portion; and

[0038] forming a third doped semiconductor portion directly on the first doped semiconductor material portion, wherein the second doped semiconductor portion and the third doped semiconductor portion have an identical composition.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] FIGS. **1-19** are sequential vertical cross-sectional views of an exemplary semiconductor structure according to the present invention at various stages of a manufacturing process.

DETAILED DESCRIPTION OF THE INVENTION

[0040] As stated above, the present invention relates to complementary metal-oxide-semiconductor (CMOS) devices having a metal gate stack transistor and a semiconductor gate stack transistor, and methods of manufacturing the same, which are now described in detail with accompanying figures. It is noted that like and corresponding elements are referred to by like reference numerals.

[0041] Referring to FIG. **1**, an exemplary semiconductor structure according to the present invention is shown, which comprises a semiconductor substrate **8** containing a substrate semiconductor layer **10** and a shallow trench isolation structure **20**. The substrate semiconductor layer **10** comprises a semiconductor material, which may be selected from, but is not limited to, silicon, germanium, silicon-germanium alloy, silicon carbon alloy, silicon-germanium-carbon alloy, gallium arsenide, indium arsenide, indium phosphide, III-V compound semiconductor materials, II-VI compound semiconductor materials, organic semiconductor materials, and other compound semiconductor materials. Typically, the semiconductor material comprises silicon. Preferably, the substrate semiconductor layer **10** is single crystalline. The semiconductor substrate **8** may be a bulk substrate, a semiconductor-on-insulator (SOI) substrate, or a hybrid substrate. The semiconductor substrate **8** may have a built-in stress in the substrate semiconductor layer **10**. While the present invention is described with a bulk substrate, implementation of the present invention on an SOI substrate or on a hybrid substrate is explicitly contemplated herein.

[0042] The shallow trench isolation structure **20** comprises a dielectric material such as silicon oxide or silicon nitride, and is formed by methods well known in the art. The exemplary semiconductor structure comprises an n-type field effect transistor (NFET) region **100**, in which an n-type metal oxide semiconductor field effect transistor (NMOSFET) is to be formed, and a p-type field effect transistor (PFET) region **200**, in which a p-type metal oxide semiconductor field effect transistor (PMOSFET) is to be formed. Each of the NFET region **100** and the PFET region **200** comprises a non-overlapping portion of a substrate semiconductor layer **10**. The portion of the substrate semiconductor layer **10** in the NFET region **100** is electrically isolated from the portion of the substrate semiconductor layer **10** in the PFET region **200**